MP8795

16V, 15A, Synchronous, Step-Down Converter with Adjustable Current Limit, Programmable Frequency

DESCRIPTION

The MP8795 is a fully integrated, high-frequency, synchronous, buck converter. It offers a very compact solution that achieves up to 15A of output current with excellent load and line regulation over a wide input supply range. The MP8795 operates at high efficiency over a wide output current load range.

The MP8795 adopts an internally compensated constant-on-time (COT) control mode that provides fast transient response and eases loop stabilization.

The operating frequency can be set to 600kHz, 800kHz, or 1000kHz easily with MODE configuration, allowing the MP8795 frequency to remain constant regardless of the input and output voltages.

The output voltage start-up ramp is controlled by an internal 1ms timer. It can be increased by adding a capacitor on SS. An open-drain power good (PGOOD) signal indicates if the output is within its nominal voltage range. PGOOD is clamped at around 0.7V with an external pull-up voltage when the input supply fails to power the MP8795.

Full protection features include over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), and over-temperature protection (OTP).

The MP8795 requires a minimal number of readily available, standard, external components and is available in a QFN-21 (3mmx4mm) package.

FEATURES

- Wide Input Voltage Range
  - 2.7V to 16V with External 3.3V VCC Bias
  - 4V to 16V with Internal Bias or External 3.3V VCC Bias
- Differential Output Voltage Remote Sense
- Programmable Accurate Current Limit Level
- 15A Output Current
- Low $R_{DS(ON)}$ Integrated Power MOSFETs
- Selectable Pulse Skip or Forced CCM Operation
- Excellent Load Regulation
- Output Voltage Discharge
- PGOOD Active Clamped at Low Level during Power Failure
- Programmable Soft-Start Time from 1ms
- Selectable Switching Frequency from 600kHz, 800kHz, and 1000kHz
- Non-Latch OCP, UVP, UVLO, Thermal Shutdown, and Latch-Off for OVP
- Output Adjustable from 0.6V to 90%*VIN, up to 5.5V Max
- Available in a QFN-21 (3mmx4mm) Package

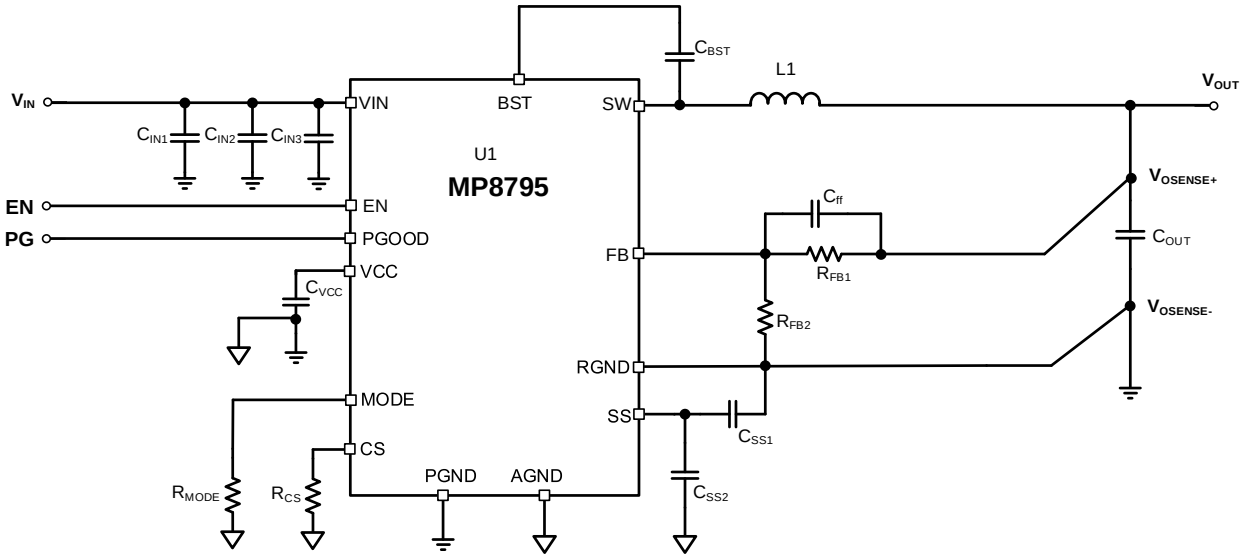
APPLICATIONS

- Solid-State Drives (SSD)
- Flat-Panel Televisions and Monitors
- Set-Top Boxes
- Distributed Power Systems

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TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
MP8795GLE*	QFN-21 (3mmx4mm)	*See Below*	1

* For Tape & Reel, add suffix –Z (e.g. MP8795GLE–Z)

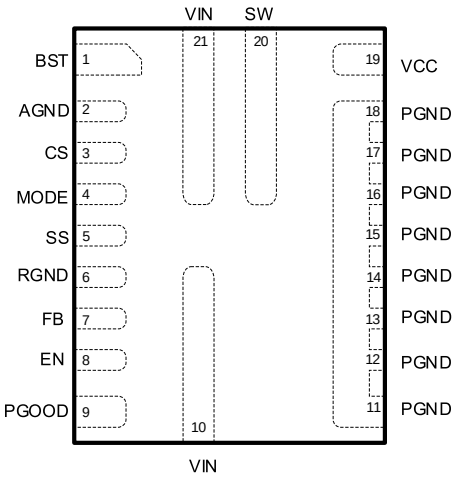
TOP MARKING

MPYW
8795
LLL
E

MP: MPS prefix
Y: Year code
W: Week code
8795: Part number
LLL: Lot number
E: Package prefix

PACKAGE REFERENCE

TOP VIEW



QFN-21 (3mmx4mm)

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ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 18V
V_{SW} (DC) ..... -0.3V to V_{IN} + 0.3V
V_{SW} (25ns) (2) ..... -5V to +25V
V_{BST} ..... V_{SW} + 4V
V_{CC}, EN 4.5V
V_{RGND} ..... ±0.3V
All other pins ..... -0.3V to +4.3V
Junction temperature ..... 170°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +170°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 4V to 16V
$V_{IN(DC)}$ - $V_{SW(DC)}$ (4) ..... -0.3V to V_{IN} + 0.3V
$V_{SW(DC)}$ (4) ..... -0.3V to V_{IN} + 0.3V
Output voltage (V_{OUT}) ..... 0.6V to 5.5V
External VCC bias (V_{CC_EXT}) ..... 3.12V to 3.6V
EN voltage (V_{EN}) 3.6V
Operating junction temp. (T_J). .. -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-21 (4mmx3mm)		
EV8795-LE-00A (5)	20	5 °C/W
JESD51-7 (6)	44	39 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) Measured using a differential oscilloscope probe.
3) The device is not guaranteed to function outside of its operating conditions.
4) The voltage rating can be in the range of -5V to +25V for a period of 25ns or less with a maximum repetition rate of 1000kHz when the input voltage is 16V.
5) Measured on EV8795-LE-00A (78mmx81mm), 4-layer PCB.
6) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C [7], typical values are tested at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Supply current (shutdown)	I_{SD}	V_{EN} = 0V		0	10	μA
Supply current (quiescent)	I_Q	V_{EN} = 2V, V_{FB} = 0.62V		650	850	μA
MOSFET						
HS switch on resistance	HS_{RDS-ON}	V_{BST-SW} = 3.3V		10		mΩ
LS switch on resistance	LS_{RDS-ON}	V_{CC} = 3.3V		3		mΩ
Switch leakage	SW_{LKG_HS}	V_{EN} = 0V, V_{SW} = 0V		0	10	μA
	SW_{LKG_LS}	V_{EN} = 0V, V_{SW} = 12V		0	30	
Current Limit						
Current limit threshold	V_{LIM}		1.15	1.2	1.25	V
I_{CS} to I_{OUT} ratio	I_{CS}/I_{OUT}	I_{OUT} ≥ 2A	9	10	11	μA/A
Switching Frequency						
Switching frequency[8]	f_{SW}	MODE = GND, I_{OUT} = 0A, V_{OUT} = 1V	480	600	720	kHz
		MODE = 30.1kΩ, I_{OUT} = 0A, V_{OUT} = 1V	680	800	920	kHz
		MODE = 60.4 kΩ, I_{OUT} = 0A, V_{OUT} = 1V	850	1000	1150	kHz
Minimum on time [8]	T_{ON_MIN}				50	ns
Minimum off time [8]	T_{OFF_MIN}				180	ns
Over-Voltage and Under-Voltage Protection						
OVP threshold	V_{OVP}		113%	116%	119%	V_{REF}
UVP threshold	V_{UVP}		77%	80%	83%	V_{REF}
Feedback Voltage and Soft Start						
Feedback voltage	V_{REF}	T_J = 25°C	594	600	606	mV
		T_J = -40°C to +125°C	591	600	609	mV
SS sourcing current	I_{SS_Source}	V_{SS} = 0V		42		μA
SS sinking current	I_{SS_Sink}	V_{SS} = 1V		12		μA
Soft-start time	t_{SS}	C_{SS} = 1nF, T_J = +25°C	0.75	1	1.25	ms
Error Amplifier						
Error amplifier offset	V_{OS}		-3	0	3	mV
Feedback current	I_{FB}	V_{FB} = V_{REF}		50	100	nA

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to +125°C (7), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Enable and UVLO						
Enable input rising threshold	VIH_{EN}		1.1	1.2	1.3	V
Enable hysteresis	V_{EN-HYS}			200		mV
Enable input current	I_{EN}	V_{EN} = 2V		0		μA
Soft shutdown discharge FET	R_{ON_DISCH}			80	150	Ω
VIN UVLO						
VIN under-voltage lockout threshold rising	VIN_{Vth_Rise}	V_{CC} = 3.3V	2.1	2.4	2.7	V
VIN under-voltage lockout threshold hysteresis	VIN_{vth_HYS}			0.55		
VCC Regulator						
VCC under-voltage lockout threshold rising	VCC_{Vth_Rise}		2.65	2.8	2.95	V
VCC under-voltage lockout threshold hysteresis	VCC_{vth_HYS}			0.3		V
VCC regulator	V_{CC}		2.88	3.00	3.12	V
VCC load regulation		Icc = 25mA		0.5		%
Power Good						
Power good high threshold	$PG_{Vth_Hi_Rise}$	FB from low to high	89.5%	92.5%	95.5%	V_{REF}
Power good low threshold	$PG_{Vth_Lo_Rise}$	FB from low to high	113%	116%	119%	V_{REF}
	$PG_{Vth_Lo_Fall}$	FB from high to low	77%	80%	83%	V_{REF}
Power good low to high delay	PG_{Td}	T_J = 25°C	0.63	0.9	1.17	ms
Power good sink current capability	V_{PG}	I_{PG} = 10mA			0.4	V
Power good leakage current	I_{PG_LEAK}	V_{PG} = 3.3V			3	μA
Power good low-level output voltage	V_{OL_100}	V_{IN} = 0V, pull PGOOD up to 3.3V through a 100kΩ resistor		650	850	mV
	V_{OL_10}	V_{IN} = 0V, pull PGOOD up to 3.3V through a 10kΩ resistor		800	1000	mV
Thermal Protection						
Thermal shutdown (7)	T_{SD}			160		°C
Thermal shutdown hysteresis (7)	T_{SD_HYS}			30		°C

Notes:

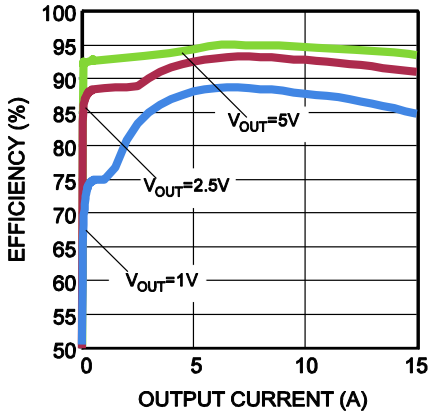
7) Derived by over-temperature correlation. Not tested in production.
8) Derived by sample characterization. Not tested in production.

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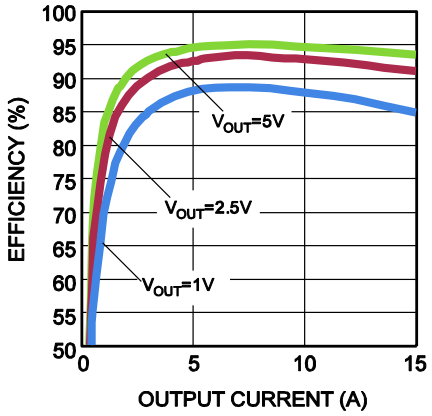
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, T_A = 25°C, V_{OUT} = 1V, f_{SW} = 800kHz, unless otherwise noted.

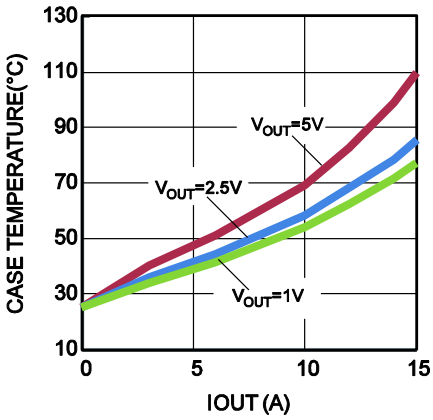
Efficiency
Pulse Skip, 0.4µH, 800kHz



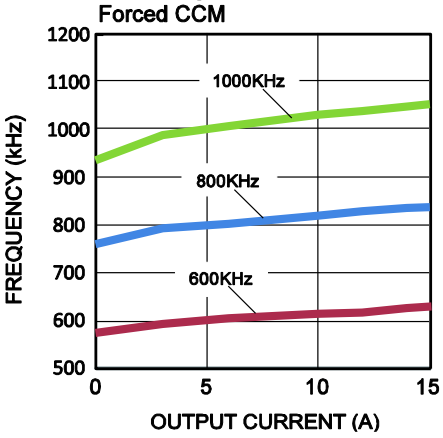
Efficiency
Forced CCM, 0.4µH, 800kHz



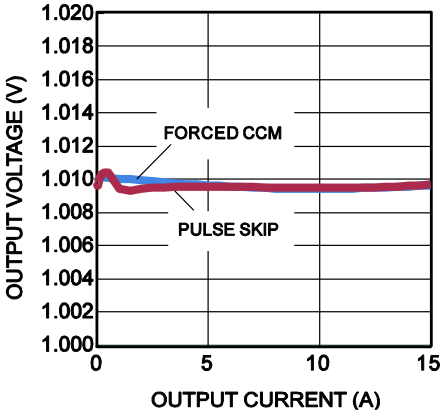
Thermal Results
800kHz



Switching Frequency vs. Output Current
Forced CCM



Output Voltage Load Regulation

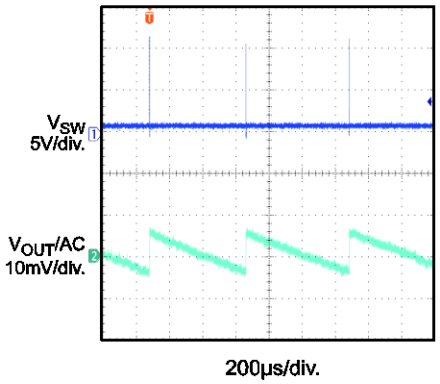


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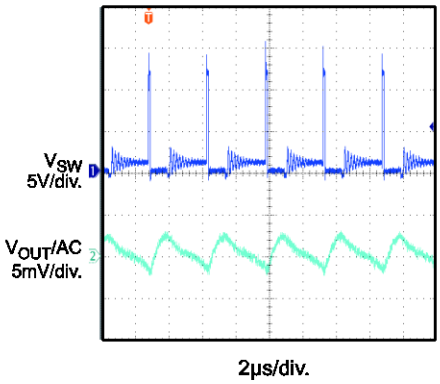
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

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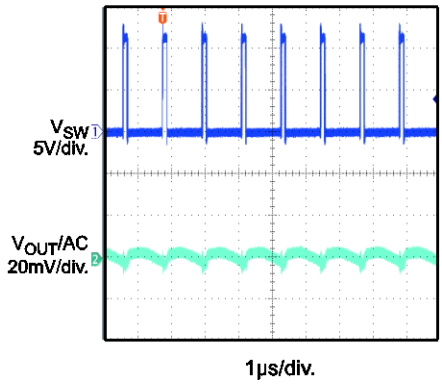
Steady State
I_{OUT} = 0A, Pulse Skip



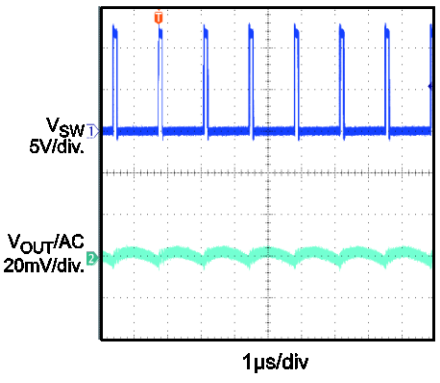
Steady State
I_{OUT} = 0.5A, Pulse Skip



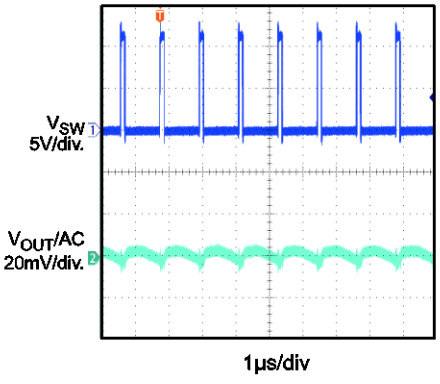
Steady State
I_{OUT} = 10A, Pulse Skip



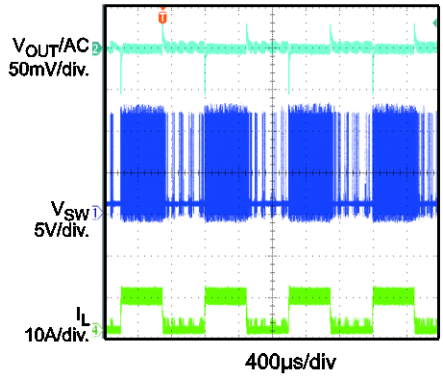
Steady State
I_{OUT} = 0A, Forced CCM



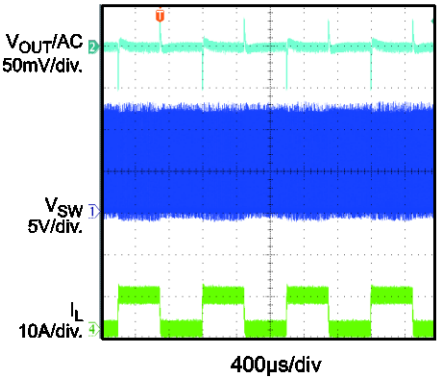
Steady State
I_{OUT} = 10A, Forced CCM



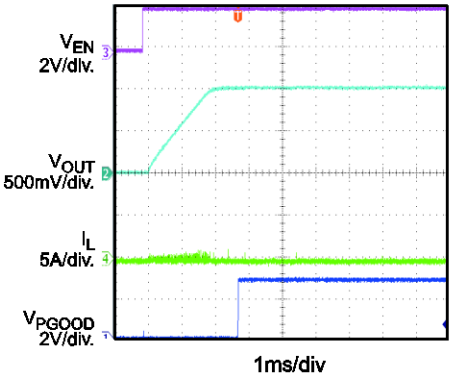
Load Transient
I_{OUT} =0A~8A, Pulse Skip



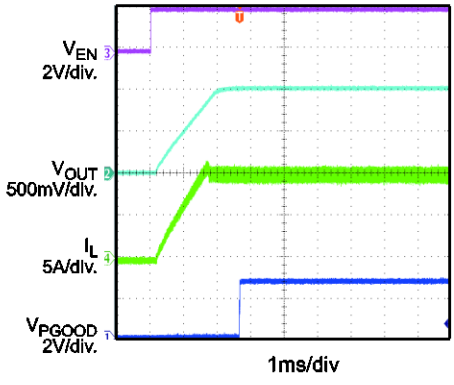
Load Transient
I_{OUT}=0A~8A, Forced CCM



Power Up through EN
I_{OUT} = 0A, Pulse Skip



Power Up through EN
I_{OUT} = 10A, Pulse Skip

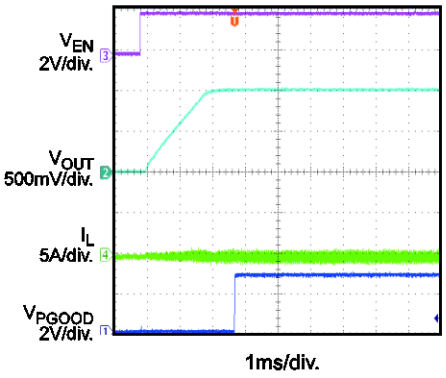


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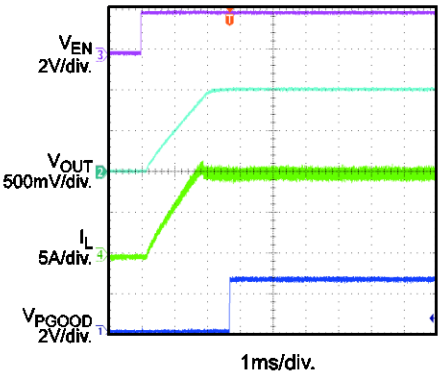
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = 25°C, V_{OUT} = 1V, f_{SW} = 800kHz, unless otherwise noted.

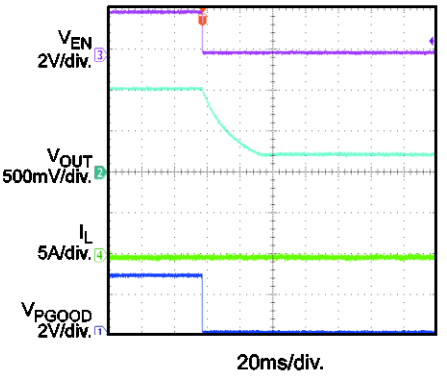
Power Up through EN
I_{OUT} = 0A, Forced CCM



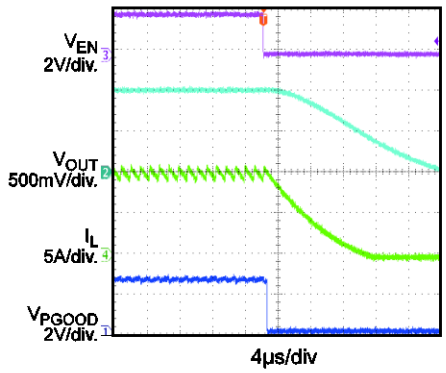
Power Up through EN
I_{OUT} = 10A, Forced CCM



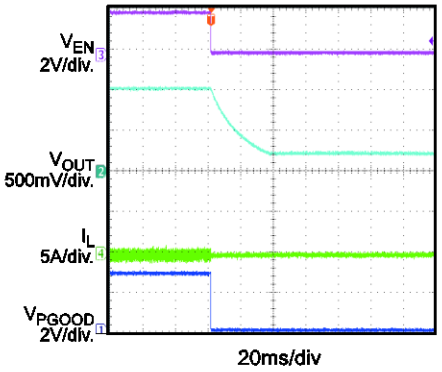
Power Down through EN
I_{OUT}=0A, Pulse Skip



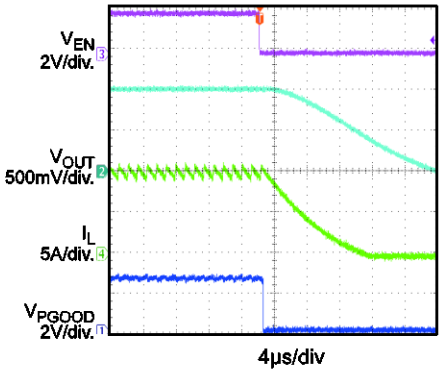
Power Down through EN
I_{OUT}=10A, Pulse Skip



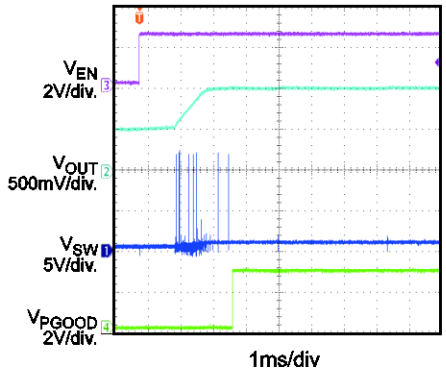
Power Down through EN
I_{OUT}=0A, Forced CCM



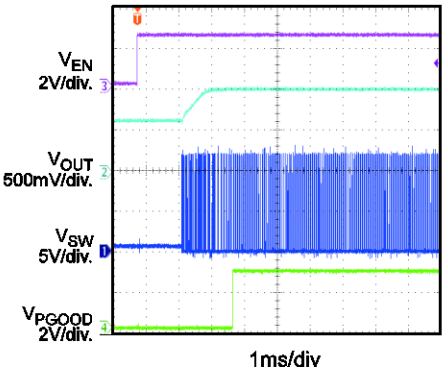
Power Down through EN
I_{OUT}=10A, Forced CCM



Pre-bias Start-Up
Pulse skip



Pre-bias Start-Up
Forced CCM



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PIN FUNCTIONS

QFN-21 PIN #	Name	Description
1	BST	**Bootstrap.** Connect a capacitor between SW and BS to form a floating supply across the high-side switch driver.
2	AGND	**Analog ground.** Select AGND as the control circuit reference point.
3	CS	**Current limit.** Connect a resistor to ground to set the current limit trip point.
4	MODE	**Operation mode selection.** Program MODE to select CCM, pulse skip mode, and the operating switching frequency. See Table 1 for additional details.
5	SS	**Soft start input.** The soft start time could be set through using different soft start capacitance. The total capacitance of C_{SS1} and C_{SS2} determines the soft-start time (t_{SS}). See Equation 2 for additional details. Minimum 1nF of both two SS capacitors (C_{SS1} from SS to RGND, C_{SS2} from SS to AGND) are always required respectively. Place SS capacitors as close to it as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics.
6	RGND	**Differential remote sense negative input.** Connect RGND to the negative side of the voltage sense point directly. Short RGND to GND if the remote sense is not used.
7	FB	**Feedback (differential remote sense positive input).** An external resistor divider from the output to RGND tapped to FB sets the output voltage. It is recommended to place the resistor divider as close to FB as possible. Vias should be avoided on the FB traces.
8	EN	**Enable.** EN is an input signal that turns the regulator on or off. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. Connect EN to VIN through a pull-up resistor or a resistive voltage divider for automatic start-up. Do not float EN.
9	PGOOD	**Power good output.** PGOOD is an open-drain signal. A pull-up resistor connected to a DC voltage is required to indicate a logic high signal if the output voltage is within regulation. There is a delay of about 1ms between the time FB ≥ 92.5% and PGOOD pulling high.
10, 21	VIN	**Input voltage.** VIN supplies power for the internal MOSFET and regulator. Input capacitors are needed to decouple the input rail. Use wide PCB traces to make the connection.
11, 12, 13, 14, 15, 16, 17, 18	PGND	**System ground.** PGND is the reference ground of the regulated output voltage. Therefore, care must be taken during PCB layout. Use wide PCB traces to make the connection.
19	VCC	**Internal 3V LDO output.** The driver and control circuits are powered from the VCC voltage. Decouple VCC with a ceramic capacitor at least 1µF placed as close to it as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics.
20	SW	**Switch output.** Connect SW to the inductor and bootstrap capacitor. SW is driven up to VIN by the high-side switch during the on-time of the PWM duty cycle. The inductor current drives SW low during the off-time. Use wide PCB traces to make the connection.

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FUNCTIONAL BLOCK DIAGRAM

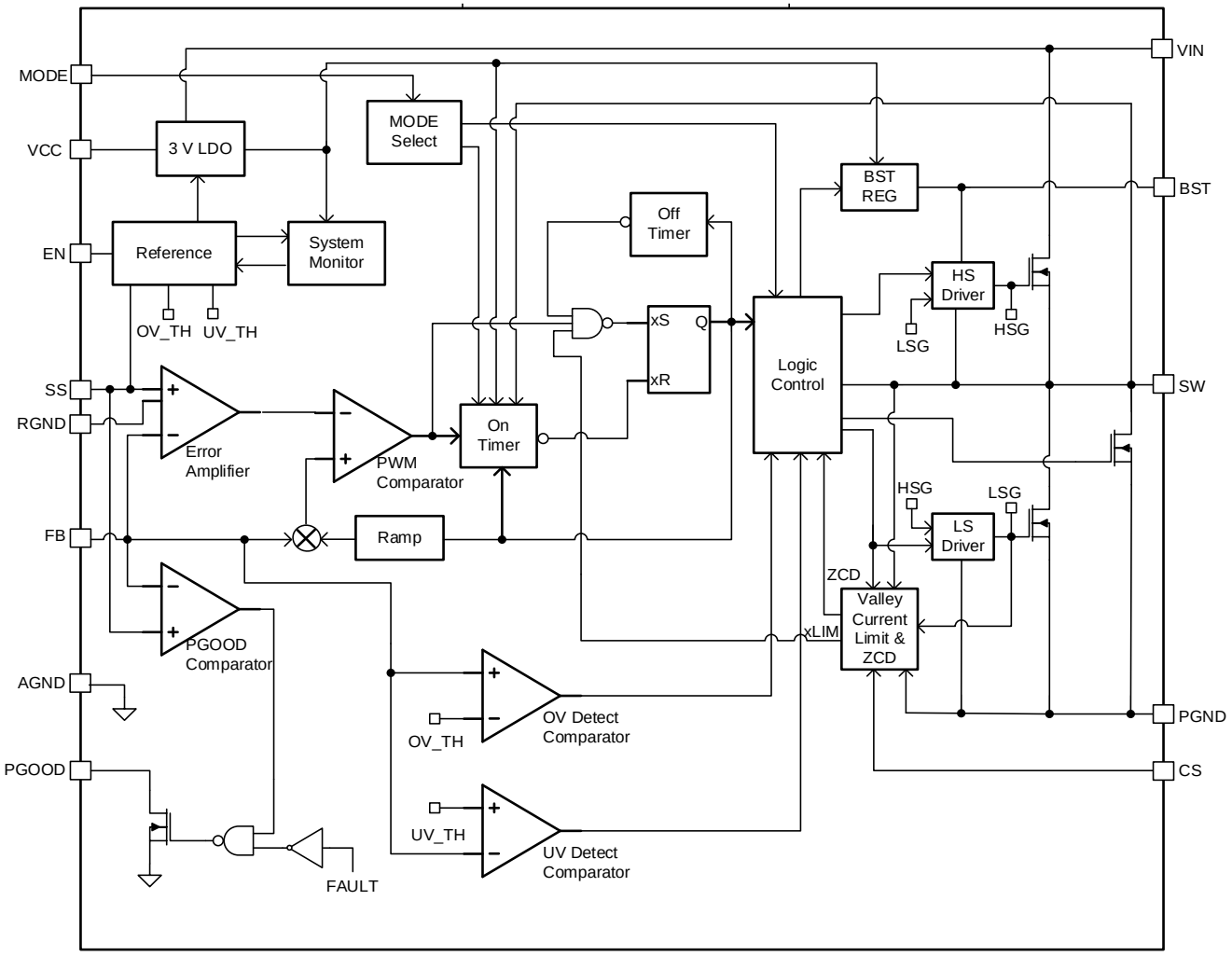


Figure 1: Functional Block Diagram

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OPERATION

COT Control

The MP8795 employs a constant-on-time (COT) control to achieve a fast load transient response. Figure 2 shows the details of the control stage of the MP8795.

The operational amplifier (AMP) corrects any error voltage between FB and VREF. The MP8795 can use AMP to provide excellent load regulation over the entire load range in either forced continuous conduction mode (CCM) or pulse skip mode.

The dedicated RGND pin helps provide the feature of the differential output voltage remote sense. The pair of the remote sense trace should be kept in low impedance to achieve the best performance.

The MP8795 has an internal RAMP compensation to support a low ESR MLCC output capacitor solution. The adaptive internal RAMP is optimized so that the MP8795 is stable in the entire operating input and output voltage ranges with a proper design of the output L/C filter.

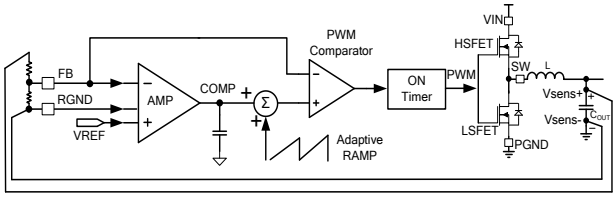


Figure 2: COT Control

PWM Operation

Figure 3 shows how the PWM signal is generated. AMP corrects any error between FB and REF and generates a fairly smooth DC voltage (COMP). The internal RAMP is superimposed onto COMP, which is compared with the FB signal. Whenever FB drops below the superimposed COMP, the integrated high-side MOSFET (HS-FET) is turned on. The HS-FET remains on for a fixed turn-on time. The fixed on time is determined by the input voltage, output voltage, and selected switching frequency. After the on period elapses, the HS-FET turns off. It turns on again when FB drops below the superimposed COMP. By repeating this operation, the MP8795 regulates the output voltage. The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is in its off state to minimize conduction loss. A dead short occurs between VIN and PGND if both the HS-FET and the LS-FET are turned on at the same time. This is called a shoot-through. To avoid a shoot-through, a dead time (DT) is generated internally between the HS-FET off and the LS-FET on period or the LS-FET off and the HS-FET on period.

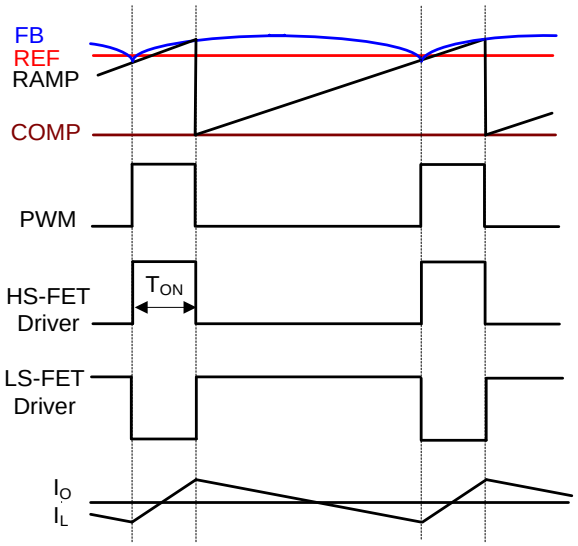


Figure 3: Heavy-Load Operation (PWM)

CCM Operation

Continuous conduction mode (CCM) occurs when the output current is high, and the inductor current is always above zero amps (see Figure 3). The MP8795 can also be configured to operate in forced CCM operation when the output current is low (see the Mode Selection section on page 14 for details).

In CCM operation, the switching frequency is fairly constant (PWM mode), hence the output ripple remains almost constant throughout the entire load range.

Pulse Skip Operation

In light-load condition, the MP8795 can be configured to work in pulse skip mode to optimize efficiency. When the load decreases, the inductor current decreases as well. Once the inductor current reaches zero, the MP8795 transitions from CCM to pulse skip mode if the MP8795 is configured in this way (see the Mode Selection section on page 14 for details).

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Figure 4 shows pulse skip mode operation at light-load condition. When FB drops below the superimposed COMP, the HS-FET turns on for a fixed interval. When the HS-FET turns off, the LS-FET turns on until the inductor current reaches zero. In pulse skip mode operation, FB does not reach superimposed COMP when the inductor current approaches zero. The LS-FET driver turns into tri-state (high-Z) when the inductor current reaches zero. A current modulator takes over the control of the LS-FET and limits the inductor current to less than -1mA. Therefore, the output capacitors discharge slowly to PGND through the LS-FET. At light-load condition, the HS-FET is not turned on as frequently in pulse skip mode as it is in forced CCM. As a result, the efficiency in pulse skip mode is improved greatly compared to that in forced CCM operation.

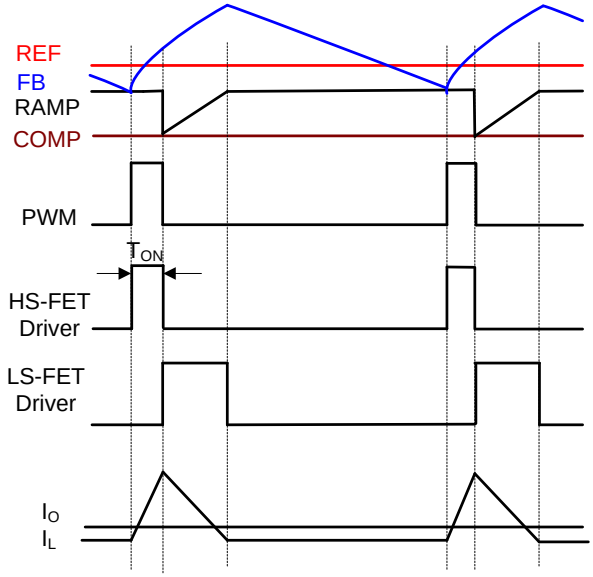


Figure 4: Pulse Skip in Light Load

As the output current increases from light load, the time period the current modulator regulates in becomes shorter. The HS-FET is turned on more frequently, and the switching frequency increases accordingly. The output current reaches critical levels when the current modulator time is zero. The critical level of the output current can be determined with Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_{SW} \times V_{IN}} \quad (1)$$

Where F_{SW} is the switching frequency.

The MP8795 enters PWM mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

The MP8795 can be configured to operate in forced CCM, even in light-load condition (see Table 1).

Mode Selection

The MP8795 provides both forced CCM operation and pulse skip mode operation in light-load condition. The MP8795 has three options for switching frequency selection. Selecting the operation mode under light-load condition and the switching frequency is done by choosing the resistance value of the resistor connected between MODE and AGND or VCC (see Table 1).

Table 1: MODE Selection

MODE	Light-Load Mode	Switching Frequency
VCC	Pulse skip	600kHz
243kΩ (±20%) to GND	Pulse skip	800kHz
121kΩ (±20%) to GND	Pulse skip	1000kHz
GND	Forced CCM	600kHz
30.1kΩ (±20%) to GND	Forced CCM	800kHz
60.4kΩ (±20%) to GND	Forced CCM	1000kHz

Soft Start (SS)

The MP8795 employs soft start (SS) to ensure a smooth output during start-up. If EN goes high, then an internal current source starts to charge the soft-start capacitors. The SS voltage (V_{SS}) overrides the REF voltage (V_{REF}) to the PWM comparator so that the output voltage smoothly ramps up as V_{SS} rises. Once V_{SS} reaches V_{REF}, V_{REF} takes over the PWM comparator. Once SS is complete, the part enters steady-state operation.

The soft-start capacitance (C_{SS}) can be calculated with Equation (2):

$$C_{SS}(nF) = \frac{t_{ss}(ms) \times 36\mu A}{0.6(V)} \quad (2)$$

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Where C_{SS} is the total capacitance of C_{SS1} and C_{SS2}. Both C_{SS1} and C_{SS2} are required to ensure V_{REF} is stable during SS.

The MP8795 has an internal minimum soft-start time (t_{SS}) (1ms). C_{SS1} and C_{SS2} should each be ≥1nF to achieve the minimum t_{SS}.

For a longer t_{SS}, see Equation 2 on page 13. For simplification, choose C_{SS2} to be 22nF, and adjust C_{SS1} to set the target V_{REF}. For example, with a 22nF C_{SS2} and 100nF C_{SS1}, t_{SS} should be 2ms.

Pre-Bias Start-Up

The MP8795 is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the IC disables switching for both the HS-FET and LS-FET until the voltage on the SS capacitor exceeds the sensed output voltage at FB. Before the SS voltage reaches the pre-biased FB level, if the BST voltage (from BST to SW) is lower than 2.3V, the LS-FET is turned on to allow the BST voltage to be charged through VCC. The LS-FET is turned on for very narrow pulses, so the drop in the pre-biased level is negligible.

Output Voltage Discharge

When the MP8795 is disabled through EN, output voltage discharge mode is enabled. This causes both the HS-FET and the LS-FET to latch off. A discharge FET connected between SW and PGND is turned on to discharge the output voltage. The typical switch on resistance of this FET is about 80Ω. Once the FB voltage drops below 20% of V_{REF}, the discharge FET is turned off.

Current Sense and Over-Current Protection (OCP)

The MP8795 features an on-die current sense and a programmable positive current limit threshold.

The current limit is active when the MP8795 is enabled. During the LS-FET on state, the SW current (inductor current) is sensed and mirrored to CS with the ratio of G_{CS}. By using a resistor (R_{CS}) from CS to AGND, the V_{CS} voltage is proportional to the SW current cycle-by-cycle. The HS-FET is only allowed to turn on when V_{CS} is below the internal OCP voltage threshold (V_{OCP}) during the LS-FET on state to limit the SW valley current cycle-by-cycle.

Calculate the current limit threshold setting from R_{CS} with Equation (3):

$$R_{CS}(\Omega) = \frac{V_{OCP}}{G_{CS} \times (I_{LIM} - \frac{(V_{IN} - V_O) \times V_O}{V_{IN}} \times \frac{1}{2 \times L \times f_s})} \quad (3)$$

Where V_{OCP} = 1.2V, G_{CS} = 10μA/A, and I_{LIM} is the desired output current limit (A).

The OCP hiccup is active 3ms after the MP8795 is enabled. Once OCP hiccup is active, if the MP8795 detects the over-current condition for 31 consecutive cycles, or if FB drops below the under-voltage protection (UVP) threshold, it enters hiccup mode. In hiccup mode, the MP8795 latches off the HS-FET immediately, and latches off the LS-FET after ZCD is detected. Meanwhile, the SS capacitor is also discharged. After about 11ms, the MP8795 attempts to soft start automatically. If the over-current condition still remains after 3ms of running, the MP8795 repeats this operation cycle until the over-current condition disappears, and the output voltage rises back to the regulation level smoothly.

Output Sinking Mode (OSM)

The MP8795 employs output sinking mode (OSM) to regulate the output voltage to the targeted value. When the FB voltage is higher than 104% of V_{REF} but is below the OVP threshold, OSM is triggered. During OSM operation, the LS-FET remains on until it reaches the -7.5A current limit. The LS-FET is then turned off momentarily for 200ns before turning on again. The MP8795 repeats this operation until FB drops below 102% of V_{REF}. The MP8795 exits OSM after 15 consecutive cycles of forced CCM.

Over-Voltage Protection (OVP)

The MP8795 monitors the output voltage by connecting FB to the tap of the output voltage feedback resistor divider to detect an over-voltage condition. This provides latch-off OVP mode.

If the FB voltage exceeds 116% of V_{REF}, the MP8795 enters latch-off OVP mode. The HS-FET latches off and PGOOD latches low until VCC or EN is recycled (turned off and turned on again). Meanwhile, the LS-FET remains on until it reaches the low-side negative current limit (NOCP). The LS-FET is then turned off momentarily for 200ns before turning on again.

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The MP8795 repeats this operation to attempt to bring down the output voltage. When the FB voltage drops below 50% of V_{REF}, the LS-FET is turned off for pulse skip mode and continues turning on for forced CCM operation. If FB rises higher than 116% V_{REF} again, the LS-FET turns on again with NOCP until FB drops back below 50% of V_{REF}. The MP8795 needs EN or VIN to recycle to clear the OVP fault.

The OVP function is enabled after SS reaches 600mV.

Over-Temperature Protection (OTP)

The MP8795 has over-temperature protection (OTP). The IC monitors the junction temperature internally. If the junction temperature exceeds the threshold value (typically 160°C), the converter shuts off and discharges the SS capacitors. This is a non-latch protection. There is a hysteresis of about 30°C. Once the junction temperature drops to about 130°C, a soft start is initiated. The OTP function is effective once the MP8795 is enabled.

Output Voltage Setting and Remote Output Voltage Sensing

First, choose a value for R1. Then R2 can be determined with Equation (4):

$$R_2(k\Omega) = \frac{V_{REF}}{V_O - V_{REF}} \times R_1(k\Omega) \quad (4)$$

To optimize the load transient response, a feed-forward capacitor (C_{FF}) is recommended to be placed in parallel with R1. R1 and C_{FF} add an extra zero to the system, which improves loop response. R1 and C_{FF} are selected so that the zero formed by R1 and C_{FF} is located around 20kHz~60kHz. Calculate this zero with Equation (5):

$$f_Z = \frac{1}{2\pi \times R1 \times C_{FF}} \quad (5)$$

Power Good (PGOOD)

The MP8795 has a power good (PGOOD) output. PGOOD is the open-drain of a MOSFET. Connect PGOOD to VCC or another external voltage source less than 3.6V through a pull-up resistor (typically 10kΩ). After applying the input voltage, the MOSFET turns on, so PGOOD is pulled to GND before SS is ready. After the FB voltage reaches 92.5% of V_{REF}, PGOOD is pulled high after a 0.8ms delay.

When the FB voltage drops to 80% of V_{REF}, or exceeds 116% of the nominal V_{REF} PGOOD is latched low. PGOOD can only be pulled high again after a new SS.

If the input supply fails to power the MP8795, PGOOD is clamped low, even though PGOOD is tied to an external DC source through a pull-up resistor. The relationship between the PGOOD voltage and the pull-up current is shown in Figure 5.

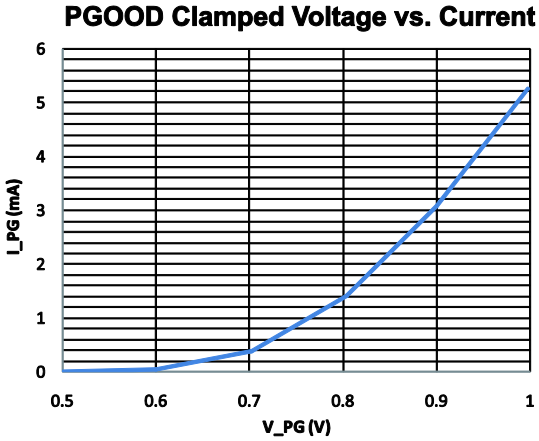


Figure 5: PGOOD Clamped Voltage vs. Pull-Up Current

Enable (EN) Configuration

The MP8795 turns on when EN goes high; the MP8795 turns off when EN goes low. EN cannot be left floating for proper operation. EN can be driven by an analog or digital control logic signal to enable or disable the MP8795.

The MP8795 provides accurate EN thresholds, so a resistor divider from VIN to AGND can be used to program the input voltage, at which the MP8795 is enabled. This is highly recommended for applications where there is no dedicated EN control logic signal to avoid possible UVLO bouncing during power-up and power-down. The resistor divider values can be determined with Equation (6):

$$V_{IN_START}(V) = VIH_{EN} \times \frac{R_{UP} + R_{DOWN}}{R_{DOWN}} \quad (6)$$

Where VIH_{EN} is 1.22V, typically.

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R_{UP} and R_{DOWN} should be chosen so that V_{EN} does not exceed 3.6V when VIN reaches the maximum value.

EN can also be connected to VIN directly through a pull-up resistor (R_{UP}). R_{UP} should be chosen so that the maximum current going to EN is 50μA. R_{UP} can be calculated with Equation (7):

$$R_{UP}(K\Omega) = \frac{VIN_{MAX}(V)}{0.05(mA)} \quad (7)$$

External VCC Bias

The MP8795 has an internal 3V LDO to power the driver and control circuits. Decouple VCC pin with a ceramic capacitor at least 1μF, and place as close to it as possible.

An external bias voltage between 3.16V to 3.6V can be applied for lower input down to 3.3V application. This can also improve the efficiency of the converter because the external bias overrides internal VCC to power on the driver and control circuits.

It's important to apply the external bias to VCC pin before VIN UVLO rising threshold or EN rising threshold comes to avoid the external bias sinking current from VCC pin.

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APPLICATION INFORMATION

Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. Use ceramic capacitors for the best performance. During layout, place the input capacitors as close to VIN as possible.

The capacitance can vary significantly with temperature. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable over a wide temperature range and offer very low ESR.

The capacitors must have a ripple current rating that exceeds the converter's maximum input ripple current. Estimate the input ripple current with Equation (8):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (8)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (9):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (9)$$

For simplification, choose an input capacitor with an RMS current rating that exceeds half the maximum load current. The input capacitor value determines the converter input voltage ripple. If there is an input voltage ripple requirement in the system, select an input capacitor that meets the specification.

Estimate the input voltage ripple with Equation (10):

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (11)$$

Output Capacitor

The output capacitor maintains the DC output voltage. Use POSCAP or ceramic capacitors. Estimate the output voltage ripple with Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}) \quad (12)$$

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency. The capacitance also dominates the output voltage ripple. For simplification, estimate the output voltage ripple with Equation (13):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (13)$$

For simplification, the output ripple can be approximated with Equation (14):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (14)$$

Inductor

The inductor supplies a constant current to the output load while being driven by the switching input voltage. A larger value inductor results in less ripple current and lower output ripple voltage, but also has a larger physical size, a higher series resistance, and a lower saturation current. Design for a peak inductor current that is below the maximum switch current limit. Calculate the inductance value with Equation (15):

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_{L}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (15)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be calculated with Equation (16):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2 \times F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (16)$$

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PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For best performance, refer to Figure 6 and follow the guidelines below.

1. Place the input MLCC capacitors as close to VIN and PGND as possible.
2. Place the major MLCC capacitors on the same layer as the MP8795.
3. Maximize the VIN and PGND copper plane to minimize the parasitic impedance.
4. Place as many PGND vias as possible as close to PGND as possible to minimize both parasitic impedance and thermal resistance.
5. Place the VCC decoupling capacitor close to the device.
6. Connect AGND and PGND at the point of the VCC capacitor's ground connection.
7. Place the BST capacitor as close to BST and SW as possible with 20 mil or wider traces to route the path. It is recommended to use a bootstrap capacitor 0.1µF to 1µF.
8. Place the REF capacitor close to SS to RGND.
9. Place via at least 10mm away from the positive side of the first input decoupling capacitor close to the IC if it must be placed on the PGOOD pad.

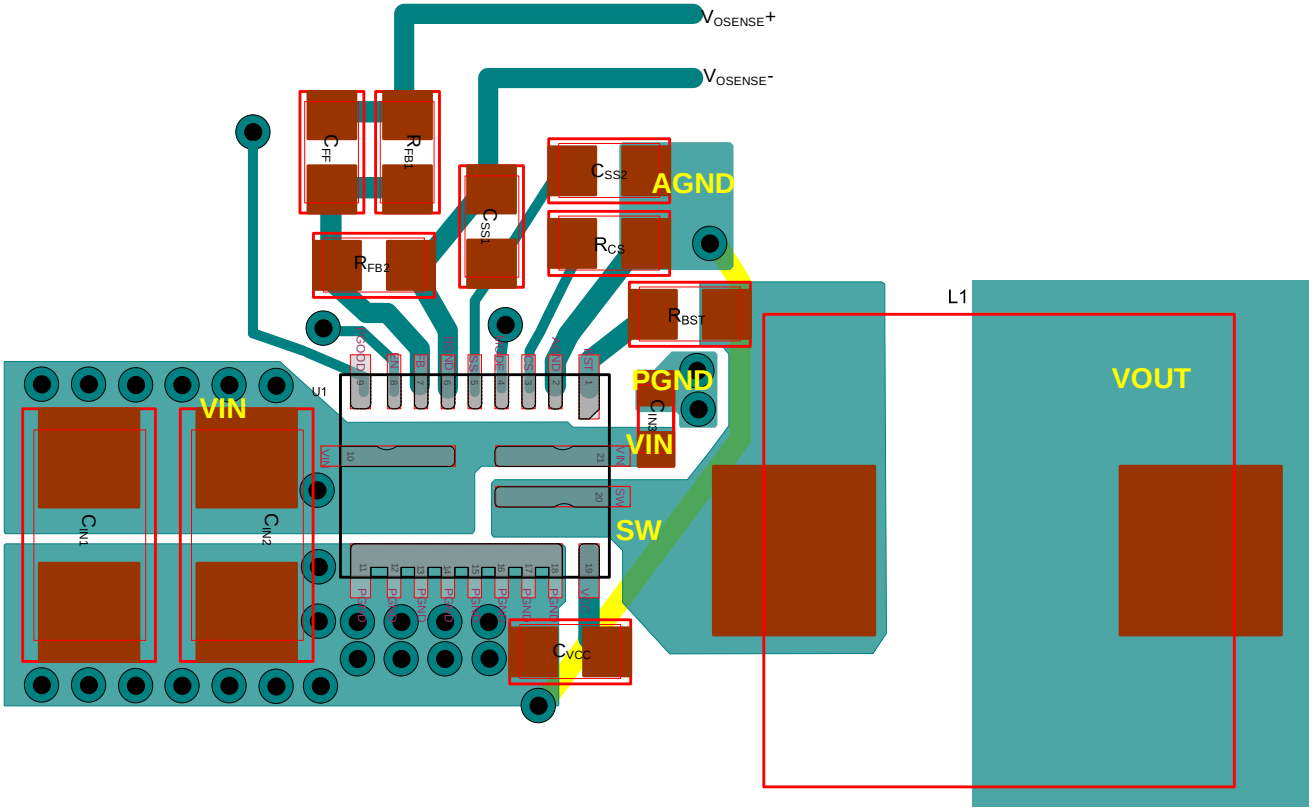


Figure 6: Recommended PCB Layout

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TYPICAL APPLICATION CIRCUIT

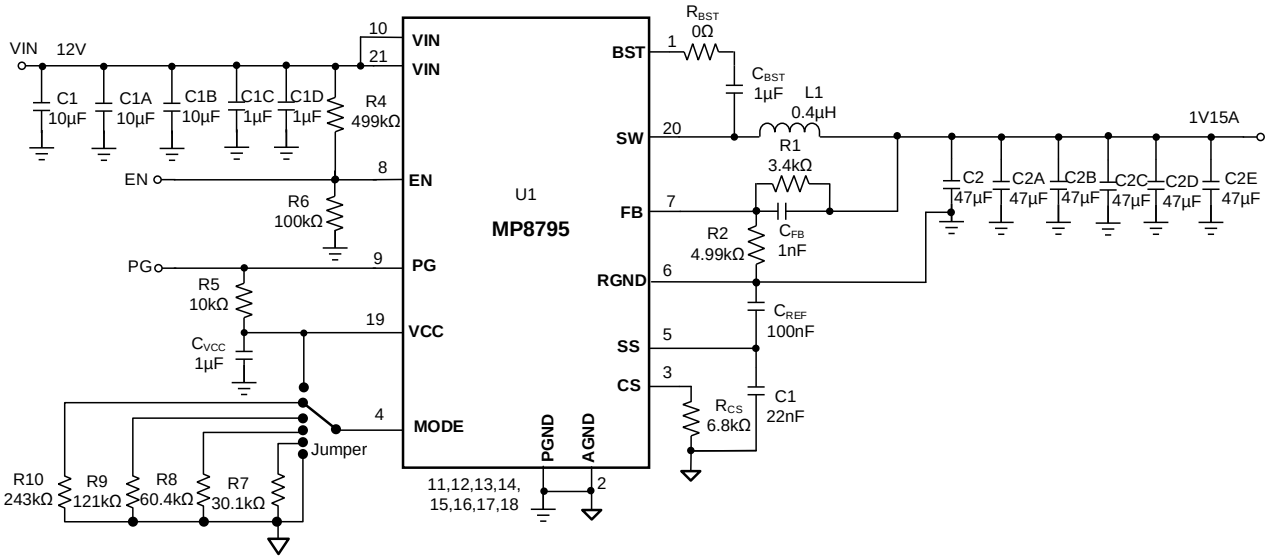
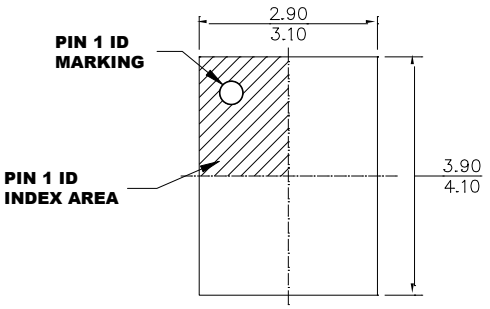


Figure 7: V_{IN} = 12V, V_{OUT} = 1V, I_{OUT} = 15A

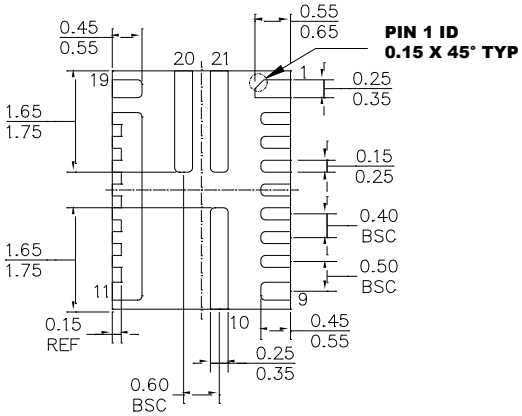
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PACKAGE INFORMATION

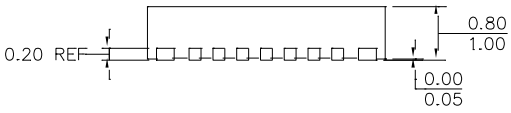
QFN-21 (3mmx4mm)



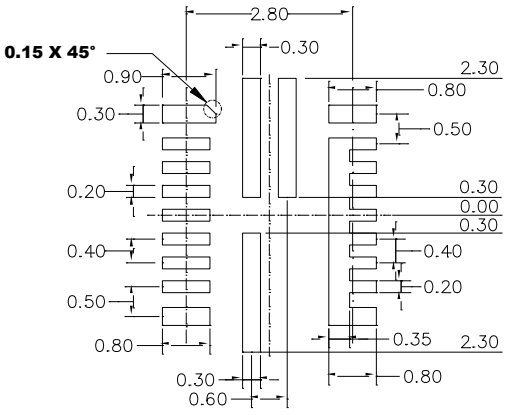
TOP VIEW



BOTTOM VIEW



SIDE VIEW



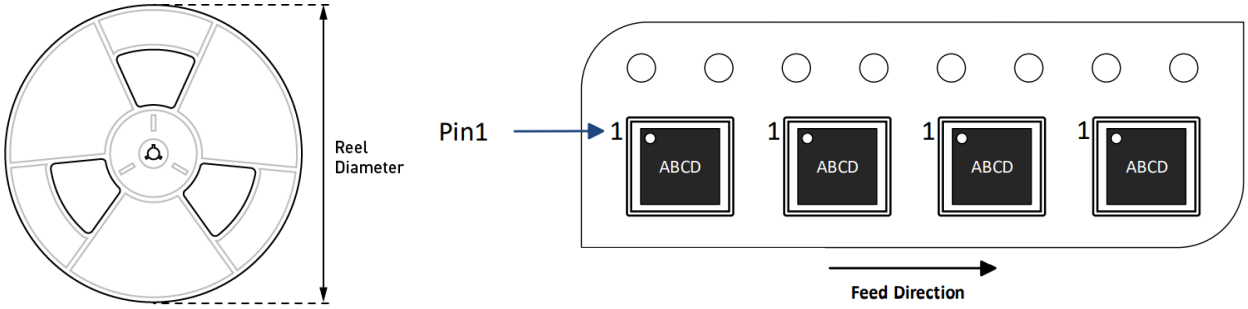
RECOMMENDED LAND PATTERN

NOTE:

1) LAND PATTERN OF PIN1,9,10,11,19,20 AND 21 HAVE THE SAME WIDTH.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
4) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-220.
6) DRAWING IS NOT TO SCALE.

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CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP8795GLE-Z	QFN-21 (3mmx4mm)	5000	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.01	9/8/2017	Initial Release	-
1.1	10/18/2022	Removed “Voltage Tracking” from the header	1
		Updated the Top Marking; added the MSL Rating; updated Pin 5 from the TRK/REF pin to the SS pin in the Package Information section	3
		Removed “V_{SW} (25ns) (2)…-3V to +25V” and updated V_{RGND} in the Absolute Maximum Ratings section; updated the Thermal Resistance section; updated Note 5; added Note 6	4
		Updated the supply current (shutdown) symbol to “I_{SD}”; updated the supply current (quiescent) symbol to “I_Q”; updated the feedback current condition to “$V_{FB} = V_{REF}$”; removed “V_{FB} = 0.5V” from the minimum on time and minimum off time conditions	5
		Updated the conditions for the Electrical Characteristics section	5–6
		Updated Note 7 and Note 8	6
		Updated the conditions for the Typical Performance Characteristics section	7–9
		Updated the SS description in the Pin Functions section	10
		Updated the section title to “Functional Block Diagram”; added “AGND” to Figure 1	11
		Updated the Soft Start (SS) section	13–14
		Added the External VCC Bias section	16
		Updated the Inductor section	17
		Added Figure 7	19
		Added the Carrier Information section	21
		Updated the footer	22
		Formatting updates	All

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